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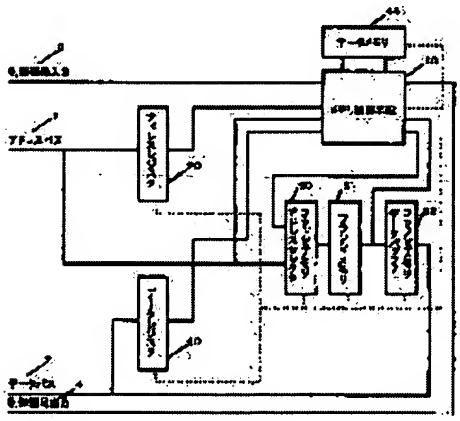
(54) FLASH MEMORY DEVICE

(57)Abstract:



PROBLEM TO BE SOLVED: To make easily executable complicated memory writing operations to a flash memory without requiring any dedicated software, by allowing a memory control means to control writing to the flash memory by blocks consisting of memory cells.

SOLUTION: The memory control means 10 holds a write address and data by controlling an address register 20 and a data register 40. The memory control means 10 controls a flash memory address selector 50 to obtain the number of a block to be written from the address that the address register 20 holds, supplies sequential addresses to the flash memory 51 through the flash memory address 50 to reads data out of the flash memory 51 with the obtained block number in order, and then stores them in a data memory 44. Further, the

control means 10 writes a command in the flash memory 51 to write new data in the flash memory 51.

LEGAL STATUS

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CLAIMS

[Claim(s)]

[Claim 1] The memory control means which is flash memory equipment which performs writing and elimination for the block which consists of two or more memory cells as a unit, and controls the whole, The address register holding the address of an address bus, and the data register holding the data of a data bus, The flash memory address selector which chooses the address of said address bus, and the address which said memory control means outputs, The flash memory which considers the address which said flash memory address selector outputs as an address input, The flash memory data buffer which connects said flash memory and said data bus, It has data memory with the memory capacity of the same magnitude as the block which is the unit which performs writing and elimination of said flash memory. Said memory control means The address of said address bus is made to supply to said flash memory through said flash memory address selector at the time of data read-out. Reading appearance of the data of the address of said address bus is carried out from said flash memory. The data by which reading appearance was carried out from said flash memory are sent out to said data bus through said flash memory data buffer. Said memory control means While making the address of said address bus hold to said address register at the time of data writing, the data of said data bus are made to hold to said data register. The block number of the block which should perform writing and elimination in said flash memory is obtained from the address made to hold to said address register. By supplying the address included in the block of this block number to said flash memory through said flash memory address selector Reading appearance of the data of each address other than the address made to hold to said address register among all the addresses of the block shown with said block number is carried out from said flash memory. It is made to write in the location corresponding to each address other than the address which held the data by which reading appearance was carried out from said flash memory to said

address register among all the addresses of said block in said data memory. It is made to write in the location corresponding to the address which made the data made to hold to said data register hold to said address register in said data memory. Flash memory equipment characterized by making the data of a block of said block number in said flash memory eliminate, and making it make the data of said data memory write in to the block of said block number in said flash memory.

[Claim 2] The memory control means which is flash memory equipment which performs writing and elimination for the block which consists of two or more memory cells as a unit, and controls the whole, The address register holding the part I part address corresponding to the block number of the block which should perform writing and elimination of the addresses which consist of the part I part address and the part II part address of an address bus, The comparator which compares with the part I part address of the addresses of said address bus the part I part address which said address register held, The flash memory address selector which chooses the address of said address bus, and the address which said memory control means outputs, The flash memory which considers the address which said flash memory address selector outputs as an address input, The flash memory data buffer which connects said flash memory and said data bus, The data memory address selector which chooses the part II part address of the addresses of said address bus, and the address for the control which said memory control means outputs, It has the storage capacity of the same magnitude as the block which is the unit which performs writing and elimination of said flash memory. The data memory to which a data flag is set corresponding to the address with which the address which said data memory address selector outputs is considered as an address input, and data are written in, It has the data memory data buffer which connects said data memory and said data bus. Said memory control means When said comparator is made to compare the address of said address bus, and the address held at said address register at the time of data read-out and an inequality output occurs from said comparator The address of said address bus is made to supply to said flash memory through said flash memory address selector. Reading appearance of the data of the address of said address bus is carried out from said flash memory. When the data by which reading appearance was carried out from said flash memory are sent out to said data bus through said flash memory data buffer and a coincidence output occurs from said comparator The part II part address of the addresses of said address bus is supplied to said data memory through said data memory address selector. When the data flag corresponding to the part II part address of the addresses of said address bus is set to said data memory, reading appearance of the data of the part II part address of the addresses of said address bus is carried out from said data memory. The data by

which reading appearance was carried out are sent out from said data memory to said data bus through said data memory data buffer. When the data flag corresponding to the part II part address of the addresses of said address bus is not set to said data memory, the address of said address bus is made to supply to said flash memory through said flash memory address selector. Reading appearance of the data of the address of said address bus is carried out from said flash memory. The data by which reading appearance was carried out from said flash memory are sent out to said data bus through said flash memory data buffer. Said memory control means While not writing in data once [after / powering on] at the time of data writing The part I part address of the addresses of said address bus is made to write in said address register. By giving the part II part address of the addresses of said address bus to said data memory through said data memory address selector While making the location corresponding to the part II part address of the addresses of said address bus of said data memory memorize the data of said data bus through said data memory data buffer The data flag corresponding to the part II part address of the addresses of said address bus is made to set. Said memory control means While writing in data once at least after powering on at the time of data writing When said comparator is made to compare the part I part address which said address register held, and the part I part address of said address bus and a coincidence output occurs from said comparator By giving the part II part address of the addresses of said address bus to said data memory through said data memory address selector While making the location corresponding to the part II part address of the addresses of said address bus of said data memory memorize the data of said data bus through said data memory data buffer When the data flag corresponding to the part II part address of the addresses of said address bus is made to set and an inequality output occurs from said comparator It lets said data memory address selector and a flash memory address selector pass for each address included in the block corresponding to the part I part address which said address register held [sequential], respectively. By giving in common to said data memory and said flash memory Data are made to copy to said data memory only about the address with which the data flag is not set by said data memory among each address included in the block corresponding to the part I part address of the addresses of said address bus in said flash memory. The data of the block corresponding to the part I part address of the addresses of said address bus in said flash memory are eliminated. The data of said data memory are made to write in the block corresponding to the part I part address of the addresses of said address bus in said flash memory. Cancel the set of the data flag of said data memory, and the part I part address of the addresses of said address bus is made to write in said address register. By giving the part II part address of the addresses of said address bus to said

data memory through said data memory address selector While making the location corresponding to the part II part address of the addresses of said address bus of said data memory memorize the data of said data bus through said data memory data buffer Flash memory equipment characterized by making it make the data flag corresponding to the part II part address of the addresses of said address bus of said data memory set.
[Claim 3] The memory control means which is flash memory equipment which performs writing and elimination for the block which consists of two or more memory cells as a unit, and controls the whole, The part II part address corresponding to the block number of the block which should perform writing and elimination of the addresses which consist of the part I part address, the part II part address, and the part III part address of an address bus, and the address which said memory control means outputs The address tag memory address selector to choose and the address tag memory to which an address tag flag is set corresponding to the address with which the address outputted from said address tag memory address selector is considered as an address input, and data are written in, The address tag memory data buffer which connects said address tag memory and said address bus, and supplies the part I part address of said address bus to said address tag memory as a data input, The comparator which compares with the part I part address of the addresses of said address bus the address by which reading appearance is carried out from said address tag memory by considering the part II part address of the addresses of said address bus as an address input, The flash memory address selector which chooses the address of said address bus, and the address which said memory control means outputs, The flash memory which considers the address outputted from said flash memory address selector as an address input, The flash memory data buffer which connects said flash memory and said data bus, The data memory address selector which chooses the part II part address of the addresses of said address bus and the part III part address, and the address for the control which said memory control means outputs, It has the same capacity as a part for the number equivalent to the magnitude of the address space of said part II part address of the block which is the unit of the writing and elimination of said flash memory. The data memory to which a data flag is set corresponding to the address with which the address which said data memory address selector outputs is considered as an address input, and data are written in, It has the data memory data buffer which connects said data memory and said data bus. Said memory control means In the time of data read-out said address tag memory address selector for the part II part address of the part I part address of the addresses of said address bus, and the addresses of said address bus as a through address input When said comparator is made to compare the data which carried out reading appearance from said address tag memory and an

inequality output occurs from said comparator The address of said address bus is made to supply to said flash memory through said flash memory address selector. Reading appearance of the data of the address of said address bus is carried out from said flash memory. When the data by which reading appearance was carried out from said flash memory are sent out to said data bus through said flash memory data buffer and a coincidence output occurs from said comparator The part II part address of the addresses of said address bus and the part III part address are supplied to said data memory through said data memory address selector. When the data flag corresponding to the part II part address of the addresses of said address bus and the part III part address is set to said data memory Reading appearance of the data of the part II part address of the addresses of said address bus and the part III part address is carried out from said data memory. being alike -- The data by which reading appearance was carried out are sent out from said data memory to said data bus through said data memory data buffer. When the data flag corresponding to the part II part address of the addresses of said address bus and the part III part address is not set to said data memory The address of said address bus is made to supply to said flash memory through said flash memory address selector. being alike -- Reading appearance of the data of the address of said address bus is carried out from said flash memory. The data by which reading appearance was carried out from said flash memory are sent out to said data bus through said flash memory data buffer. Said memory control means Before completing the writing to all the addresses of said address tag memory at the time of data writing While considering said address tag memory address selector for the part II part address of the addresses of said address bus as a through address input and making it write in said address tag memory by making the part I part address of the addresses of said address bus into a data input The address tag flag corresponding to the address which performed the data writing in said address tag memory is made to set. By giving the part II part address of the addresses of said address bus, and the part III part address to said data memory through said data memory address selector While making the location corresponding to the part II part address of the addresses of said address bus of said data memory, and the part III part address memorize the data of said data bus through said data memory data buffer The data flag corresponding to the part II part address of the addresses of said address bus in said data memory and the part III part address is made to set. Said memory control means After the writing to all the addresses of said address tag memory is completed and all the address tag flags of all of said address tag memory that carried out the address mapping are set at the time of data writing Said comparator is made to compare the data which carried out reading appearance from said address tag memory by considering the part II part address of the

part I part address of the addresses of said address bus, and the addresses of said address bus as an address input. When a coincidence output occurs from said comparator, it is said data memory address selector about the part II part address of the addresses of said address bus, and the part III part address. While making the location corresponding to the part II part address of the addresses of said address bus of said data memory, and the part III part address memorize the data of said data bus through said data memory data buffer by letting it pass and giving to said data memory The data flag corresponding to the part II part address of the addresses of said address bus of said data memory and the part III part address is made to set. When an inequality output occurs from said comparator With the data which all the addresses and those addresses of said address tag memory were made to memorize It lets said data memory address selector and a flash memory address selector pass for each address included in the block of the number corresponding to two or more sets of part I part addresses and the part II part address which are decided, respectively [sequential], respectively. By giving in common to said data memory and said flash memory Only about the address with which the data flag is not set by said data memory among each address included in the block of the number corresponding to two or more sets of part I part addresses in the address of said address bus in said flash memory, and the part II part address, data Make it copy to said data memory, and the data of the block corresponding to two or more sets of part I part addresses and the part II part address which are decided, respectively with the data which all the addresses and those addresses of said address tag memory were made to memorize are eliminated. The data of said data memory are made to write in the block corresponding to two or more sets of part I part addresses in the address of said address bus in said flash memory, and the part II part address. Until it cancels the set of the data flag of said data memory and completes the writing to all the addresses of said address tag memory While considering said address tag memory address selector for the part II part address of the addresses of said address bus as a through address input and making it write in said address tag memory by making the part I part address of the addresses of said address bus into a data input The address tag flag corresponding to the address which performed the data writing in said address tag memory is made to set. By giving the part II part address of the addresses of said address bus, and the part III part address to said data memory through said data memory address selector While making the location corresponding to the part II part address of the addresses of said address bus of said data memory, and the part III part address memorize the data of said data bus through said data memory data buffer Flash memory equipment characterized by making it make the data flag corresponding to the part II part address of the addresses of said address bus in said data memory, and

the part III part address set.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to memory apparatus, such as a personal computer and a Personal Digital Assistant.

[0002]

[Description of the Prior Art] Conventionally, using a dynamic RAM and a static RAM as main storage, such as a personal computer and a Personal Digital Assistant, one approach continued energization to the memory apparatus, even if the power source was disconnected, and it held data. Another had a method of using nonvolatile memory, such as a flash plate RAM.

[0003]

[Problem(s) to be Solved by the Invention] By the 1st approach in the above-mentioned conventional approach, in order to have to continue feed to memory, before the cell was lost, charge and exchange of a cell had to be carried out. However, since there was consumption of a cell also when not using a device, it had the danger that a cell would be lost during an intact period, therefore data would be destroyed. Moreover, in order to have to supply a power source to memory also to exchange of a cell, the device of building in a small cell was required.

[0004] By the 2nd approach, since it was unnecessary in the feed to the memory in the condition of having disconnected the power source, although the danger of being based on the 1st approach disappeared, there were some limits according to the capacity of a flash memory. Although the read-out rate had the usual memory and the speed which is not inferiority, the flash memory needed to require time amount for writing, and needed to perform write-in actuation with the special mode. In order to avoid this limit, the software of dedication, like basic software (OS) manages a flash memory was required. In addition, since the write-in time amount over a flash memory was long, it also had the trouble that the engine performance fell to general memory again.

[0005] This invention does not solve the above-mentioned trouble for using a flash memory as main storage, such as a personal computer and a Personal Digital Assistant, and it aims at offering the flash memory equipment which can write in without needing

the software of dedication. In addition, it aims at offering the flash memory equipment to which it writes and degradation by time amount is made as for things few.

[0006]

[Means for Solving the Problem] The memory control means which flash memory equipment according to claim 1 is flash memory equipment which performs writing and elimination for the block which consists of two or more memory cells as a unit, and controls the whole, The address register holding the address of an address bus, and the data register holding the data of a data bus, The flash memory address selector which chooses the address of an address bus, and the address which a memory control means outputs, The flash memory which considers the address which a flash memory address selector outputs as an address input, The flash memory data buffer which connects a flash memory and a data bus, It has data memory with the memory capacity of the same magnitude as the block which is the unit which performs writing and elimination of a flash memory. A memory control means The address of an address bus is made to supply to a flash memory through a flash memory address selector at the time of data read-out. Reading appearance of the data of the address of an address bus is carried out from a flash memory. The data by which reading appearance was carried out from the flash memory are sent out to a data bus through a flash memory data buffer. A memory control means While making the address of an address bus hold to an address register at the time of data writing, the data of a data bus are made to hold to a data register. The block number of the block which should perform writing and elimination in a flash memory is obtained from the address made to hold to an address register. By supplying the address included in the block of this block number to a flash memory through a flash memory address selector Reading appearance of the data of each address other than the address made to hold to an address register among all the addresses of the block shown with a block number is carried out from a flash memory. It is made to write in the location corresponding to each address other than the address which held the data by which reading appearance was carried out from the flash memory to the address register among all the addresses of the block in data memory. It is made to write in the location corresponding to the address which made the data made to hold to a data register hold to the address register in data memory. The data of a block of the block number in a flash memory are made to eliminate, and it is characterized by making it make the data of data memory write in to the block of the block number in a flash memory.

[0007] Since the writing to a flash memory was controlled by the memory control means according to this configuration, complicated memory write-in actuation to a flash memory can be performed easily, without needing the software of dedication, and

treating like the usual memory is possible. The memory control means which flash memory equipment according to claim 2 is flash memory equipment which performs writing and elimination for the block which consists of two or more memory cells as a unit, and controls the whole, The address register holding the part I part address corresponding to the block number of the block which should perform writing and elimination of the addresses which consist of the part I part address and the part II part address of an address bus, The comparator which compares with the part I part address of the addresses of an address bus the part I part address which the address register held, The flash memory address selector which chooses the address of an address bus, and the address which a memory control means outputs, The flash memory which considers the address which a flash memory address selector outputs as an address input, The flash memory data buffer which connects a flash memory and a data bus, The data memory address selector which chooses the part II part address of the addresses of an address bus, and the address for the control which a memory control means outputs, It has the storage capacity of the same magnitude as the block which is the unit which performs writing and elimination of a flash memory. The data memory to which a data flag is set corresponding to the address with which the address which a data memory address selector outputs is considered as an address input, and data are written in, It has the data memory data buffer which connects data memory and a data bus. A memory control means When a comparator is made to compare the address of an address bus, and the address held at the address register at the time of data read-out and an inequality output occurs from a comparator The address of an address bus is made to supply to a flash memory through a flash memory address selector. Reading appearance of the data of the address of an address bus is carried out from a flash memory. When the data by which reading appearance was carried out from the flash memory are sent out to a data bus through a flash memory data buffer and a coincidence output occurs from a comparator The part II part address of the addresses of an address bus is supplied to data memory through a data memory address selector. When the data flag corresponding to the part II part address of the addresses of an address bus is set to data memory, reading appearance of the data of the part II part address of the addresses of an address bus is carried out from data memory. The data by which reading appearance was carried out are sent out from data memory to a data bus through a data memory data buffer. When the data flag corresponding to the part II part address of the addresses of an address bus is not set to data memory, the address of an address bus is made to supply to a flash memory through a flash memory address selector. Reading appearance of the data of the address of an address bus is carried out from a flash memory. The data by which reading appearance was carried out from the

flash memory are sent out to a data bus through a flash memory data buffer. A memory control means While not writing in data once [after / powering on] at the time of data writing The part I part address of the addresses of an address bus is made to write in an address register. By giving the part II part address of the addresses of an address bus to data memory through a data memory address selector While making the location corresponding to the part II part address of the addresses of the address bus of data memory memorize the data of a data bus through a data memory data buffer The data flag corresponding to the part II part address of the addresses of an address bus is made to set. A memory control means While writing in data once at least after powering on at the time of data writing When a comparator is made to compare the part I part address and the part I part address of an address bus which the address register held and a coincidence output occurs from a comparator By giving the part II part address of the addresses of an address bus to data memory through a data memory address selector While making the location corresponding to the part II part address of the addresses of the address bus of data memory memorize the data of a data bus through a data memory data buffer When the data flag corresponding to the part II part address of the addresses of an address bus is made to set and an inequality output occurs from a comparator By giving in common each address included in the block corresponding to the part I part address which the address register held to data memory and a flash memory respectively through a data memory address selector and a flash memory address selector [sequential] Data are made to copy to data memory only about the address with which the data flag is not set by data memory among each address included in the block corresponding to the part I part address of the addresses of the address bus in a flash memory. The data of the block corresponding to the part I part address of the addresses of the address bus in a flash memory are eliminated. The data of data memory are made to write in the block corresponding to the part I part address of the addresses of the address bus in a flash memory. Cancel the set of the data flag of data memory and the part I part address of the addresses of an address bus is made to write in an address register. By giving the part II part address of the addresses of an address bus to data memory through a data memory address selector While making the location corresponding to the part II part address of the addresses of the address bus of data memory memorize the data of a data bus through a data memory data buffer It is characterized by making it make the data flag corresponding to the part II part address of the addresses of the address bus of data memory set.

[0008] Since the writing to a flash memory was controlled by the memory control means according to this configuration, complicated memory write-in actuation to a flash memory can be performed easily, without needing the software of dedication, and

treating like the usual memory is possible. And it completes in writing once to the continuous writing to the same block, and write-in time amount can be shortened.

[0009] The memory control means which flash memory equipment according to claim 3 is flash memory equipment which performs writing and elimination for the block which consists of two or more memory cells as a unit, and controls the whole, The part II part address corresponding to the block number of the block which should perform writing and elimination of the addresses which consist of the part I part address, the part II part address, and the part III part address of an address bus, and the address which a memory control means outputs The address tag memory address selector to choose and the address tag memory to which an address tag flag is set corresponding to the address with which the address outputted from an address tag memory address selector is considered as an address input, and data are written in, The address tag memory data buffer which connects address tag memory and an address bus and supplies the part I part address of an address bus to address tag memory as a data input, The comparator which compares with the part I part address of the addresses of an address bus the address by which reading appearance is carried out from address tag memory by considering the part II part address of the addresses of an address bus as an address input, The flash memory address selector which chooses the address of an address bus, and the address which a memory control means outputs, The flash memory which considers the address outputted from a flash memory address selector as an address input, The flash memory data buffer which connects a flash memory and a data bus, The data memory address selector which chooses the part II part address of the addresses of an address bus and the part III part address, and the address for the control which a memory control means outputs, It has the same capacity as a part for the number equivalent to the magnitude of the address space of the part II part address of the block which is the unit of the writing and elimination of a flash memory. The data memory to which a data flag is set corresponding to the address with which the address which a data memory address selector outputs is considered as an address input, and data are written in, It has the data memory data buffer which connects data memory and a data bus. A memory control means A comparator is made to compare the data to which reading appearance of the address tag memory address selector was carried out for the part II part address of the part I part address of the addresses of an address bus, and the addresses of an address bus from address tag memory as a through address input at the time of data read-out. When an inequality output occurs from a comparator, the address of an address bus is made to supply to a flash memory through a flash memory address selector. Reading appearance of the data of the address of an address bus is carried out from a flash memory. When the data by which reading appearance

was carried out from the flash memory are sent out to a data bus through a flash memory data buffer and a coincidence output occurs from a comparator The part II part address of the addresses of an address bus and the part III part address are supplied to data memory through a data memory address selector. When the data flag corresponding to the part II part address of the addresses of an address bus and the part III part address is set to data memory, reading appearance of the data of the part II part address of the addresses of an address bus and the part III part address is carried out from data memory. The data by which reading appearance was carried out are sent out from data memory to a data bus through a data memory data buffer. When the data flag corresponding to the part II part address of the addresses of an address bus and the part III part address is not set to data memory, the address of an address bus is made to supply to a flash memory through a flash memory address selector. Reading appearance of the data of the address of an address bus is carried out from a flash memory. The data by which reading appearance was carried out from the flash memory are sent out to a data bus through a flash memory data buffer. A memory control means Before completing the writing to all the addresses of address tag memory at the time of data writing While considering an address tag memory address selector for the part II part address of the addresses of an address bus as a through address input and making it write in address tag memory by making the part I part address of the addresses of an address bus into a data input The address tag flag corresponding to the address which performed the data writing in address tag memory is made to set. By giving the part II part address of the addresses of an address bus, and the part III part address to data memory through a data memory address selector While making the location corresponding to the part II part address of the addresses of the address bus of data memory, and the part III part address memorize the data of a data bus through a data memory data buffer The data flag corresponding to the part II part address of the addresses of the address bus in data memory and the part III part address is made to set. A memory control means After the writing to all the addresses of address tag memory is completed and all the address tag flags of all of address tag memory that carried out the address mapping are set at the time of data writing A comparator is made to compare the data which carried out reading appearance from address tag memory by considering the part II part address of the part I part address of the addresses of an address bus, and the addresses of an address bus as an address input. When a coincidence output occurs from a comparator By giving the part II part address of the addresses of an address bus, and the part III part address to data memory through a data memory address selector While making the location corresponding to the part II part address of the addresses of the address bus of data memory, and the part III

part address memorize the data of a data bus through a data memory data buffer When the data flag corresponding to the part II part address of the addresses of the address bus of data memory and the part III part address is made to set and an inequality output occurs from a comparator It is a data memory ad to sequential community about each address included in the block of the number corresponding to two or more sets of part I part addresses and the part II part address which are decided, respectively with the data which all the addresses and those addresses of address tag memory were made to memorize. By giving in common to data memory and a flash memory respectively through a loess selector and a flash memory address selector Only about the address with which the data flag is not set by data memory among each address included in the block of the number corresponding to two or more sets of part I part addresses in the address of the address bus in a flash memory, and the part II part address, data Make it copy to data memory and the data of the block corresponding to two or more sets of part I part addresses and the part II part address which are decided, respectively with the data which all the addresses and those addresses of address tag memory were made to memorize are eliminated. The data of data memory are made to write in the block corresponding to two or more sets of part I part addresses in the address of the address bus in a flash memory, and the part II part address. Until it cancels the set of the data flag of data memory and completes the writing to all the addresses of address tag memory While considering an address tag memory address selector for the part II part address of the addresses of an address bus as a through address input and making it write in address tag memory by making the part I part address of the addresses of an address bus into a data input The address tag flag corresponding to the address which performed the data writing in address tag memory is made to set. By giving the part II part address of the addresses of an address bus, and the part III part address to data memory through a data memory address selector While making the location corresponding to the part II part address of the addresses of the address bus of data memory, and the part III part address memorize the data of a data bus through a data memory data buffer It is characterized by making it make the data flag corresponding to the part II part address of the addresses of the address bus in data memory, and the part III part address set.

[0010] Since the writing to a flash memory was controlled by the memory control means according to this configuration, complicated memory write-in actuation to a flash memory can be performed easily, without needing the software of dedication, and treating like the usual memory is possible. And it completes in writing once to the continuous writing to two or more blocks, and write-in time amount can be shortened further.

[0011]

[Embodiment of the Invention] Hereafter, the gestalt of operation of the flash memory equipment of this invention is explained to a detail using drawing.

(The gestalt of the 1st operation; it corresponds to claim 1) Drawing 1 is the block diagram showing the configuration of the flash memory equipment in the gestalt of operation of the 1st of this invention. drawing 1 -- setting -- 1 -- an address bus and 2 -- a data bus and 3 -- a control signal input and 4 -- a control signal output and 10 -- for a data register and 44, as for a flash memory address selector and 51, data memory and 50 are [a memory control means and 20 / an address register and 40 / a flash memory and 52] flash memory data buffers.

[0012] This flash memory equipment performs writing and elimination for the block which consists of two or more memory cells as a unit. In this, the address register 20 with which the memory control means 10 controls the whole holds the address of an address bus 1. A data register 40 holds the data of a data bus 2. The flash memory address selector 50 chooses the address of an address bus 1, and the address which the memory control means 10 outputs. A flash memory 51 considers the address which the flash memory address selector 50 outputs as an address input. The flash memory data buffer 52 connects a flash memory 51 and a data bus 2. Data memory 44 has the storage capacity of the same magnitude as the block which is the unit which performs writing and elimination of a flash memory 51.

[0013] Here, the memory control means 10 sends out the data by which were made to supply the address of an address bus 1 to a flash memory 51 through the flash memory address selector 50 at the time of data read-out, and were made to carry out reading appearance of the data of the address of an address bus 1 from a flash memory 51, and reading appearance was carried out from the flash memory 51 to a data bus 2 through the flash memory data buffer 52. Moreover, the memory control means 10 makes the data of a data bus 2 hold to a data register 40 while making the address of an address bus 1 hold to an address register 20 at the time of data writing. The block number of the block which should perform writing and elimination in a flash memory 51 is obtained from the address made to hold to an address register 20. By supplying the address included in the block of this block number to a flash memory 51 through the flash memory address selector 50 Reading appearance of the data of each address other than the address made to hold to an address register 20 among all the addresses of the block shown with a block number is carried out from a flash memory 51. It is made to write in the location corresponding to each address other than the address which held the data by which reading appearance was carried out from the flash memory 51 to the address register 20 among all the addresses of the block in data memory 44. It is made to write

in the location corresponding to the address which made the data made to hold to a data register 40 hold to the address register 20 in data memory 44. He makes the data of a block of the block number in a flash memory 51 eliminate, and is trying to make the data of data memory 44 write in to the block of the block number in a flash memory 51.

[0014] hereafter, referring to drawing 1 , reading appearance of the actuation of the gestalt of this operation is carried out, and reading appearance is carried out in the middle of writing and write-in, or it divides and explains to writing. In this drawing, the broken line shows the signal for control. First, read-out is explained. The address signal of an address bus 1 is added to a flash memory 51 through the flash memory address selector 50 at the time of read-out. A flash memory 51 outputs the data of the added address, and outputs data to a data bus 2 through the flash memory data buffer 52. The memory control means 10 controls the selection direction of the flash memory address selector 50, and the flash memory data buffer 52. In this case, it becomes simple memory read-out.

[0015] Then, writing is explained. Writing can be decomposed into four phases. The 1st is the phase required of the address register 20 and the data register 40 of writing in and holding the address and data. The memory control means 10 controls an address register 20 and a data register 40, and makes the content of an address bus 1 and the data bus 2 hold, respectively. The actuation to the exterior as a memory apparatus can be completed now. Therefore, it is visible as simple memory from the side using memory apparatus, such as a microcomputer.

[0016] The 2nd phase is a phase of moving the data of the block in a flash memory 51 to rewrite to data memory 44. The memory control means 10 controls the flash memory address selector 50, and lets the signal which the memory control means 10 outputs pass. The memory control means 10 obtains the number of the block rewritten from the address which an address register 20 holds. By giving the address serially to a flash memory 51 through a flash memory address selector, the memory control means 10 reads the data of the flash memory 51 of the obtained block number one by one, and stores them in data memory 44. The content of the data register 40 is stored in the data memory 44 equivalent to the address of an address register 20. Now, the earlier data which suited the flash memory 51, and the newly rewritten data were held at data memory 44.

[0017] The 3rd phase is a phase which eliminates the block which should rewrite a flash memory 51. This can be performed because the memory control means 10 writes in a command to a flash memory 51. Control of the flash memory address selector 50 is the same as the 2nd phase. The 4th phase is a phase which writes in new data to a flash memory 51. This as well as the 3rd step can be performed because the memory control

means 10 writes in a command to a flash memory 51. Thus, the block with which the data to rewrite are contained can be transposed to a new content.

[0018] Here, explanation is added about the control approach of a general flash memory. A flash memory can perform elimination and rewriting of the content. In order to perform elimination and rewriting of the content, a memory chip goes into washout mode or a write mode by writing specific data to the specific address of a flash memory. If a command is written in, it will express writing specific data to the specific address. If it goes into washout mode or a write mode, specified processing will be performed a flash memory not being visible as a ROM, and it being visible like an I/O device, and exchanging information with a memory control means.

[0019] Below, read-out or the writing in the middle of write-in is explained. Since it cannot answer in the middle of write-in to the memory access from the outside, the response to memory access is kept waiting with the control signal output 4. As soon as writing is completed, it reads, or write-in actuation is started, and the response of memory access is made to complete. Before performing powering off, the data which remain in the address register 20 and the data register 40 must be written in to a flash memory 51. The procedure of writing is the same as that of what was explained in the top.

[0020] As mentioned above, since according to the gestalt of this operation an address register 20, a data register 40, the flash memory address selector 51, and data memory 44 are formed and the writing to a flash memory 51 was controlled by the memory control means 10, complicated memory write-in actuation to a flash memory 51 can be performed easily, without needing the software of dedication, and treating like the usual memory is possible. Therefore, it can access without being conscious of a flash memory 51, and the software created for the memory of the general result can be worked as it is.

[0021] (The gestalt of the 2nd operation; it corresponds to claim 2) Drawing 2 R> 2 is the block diagram showing the configuration of the flash memory equipment in the gestalt of operation of the 2nd of this invention. drawing 2 -- setting -- 1 -- an address bus and 2 -- a data bus and 3 -- a control signal input and 4 -- a control signal output and 11 -- a memory control means and 20 -- an address register and 30 -- for data memory and 43, as for a flash memory address selector and 51, a data memory data buffer and 50 are [a comparator and 41 / a data memory address selector and 42 / a flash memory and 52] flash memory data buffers.

[0022] Drawing 4 is the schematic diagram showing the data bit configuration of data memory 42. In drawing 4 , 60 is data division and 61 is the data flag section. First, explanation is added about data memory 42. Data memory 42 has the same address space as one block of a flash memory 51. The configuration of data memory 42 is

explained referring to drawing 4 . Data memory 42 consists of data division 60 and the data flag section 61. Data division 60 can store the data which should update a flash memory 51, can read them by the address bus 1 and the data bus 2, or the memory control means 11, and can be written in. The data flag section 61 can show that data are set, can read it only by the memory control means 11, and can be written in. Moreover, if writing is performed from an address bus 1 and a data bus 2, the data flag section 61 of the corresponding address will be set. In addition, the after [powering on] data flag section 61 is taken as the condition that all are not set.

[0023] Below, flash memory equipment is explained. This flash memory equipment performs writing and elimination for the block which consists of two or more memory cells as a unit. In this, the memory control means 11 controls the whole. An address register 20 holds the part I part address corresponding to the block number of the block which should perform writing and elimination of the addresses which consist of the part I part address (upper address) and the part II part address (lower address) of an address bus 1. A comparator 30 compares with the part I part address of the addresses of an address bus 1 the part I part address which the address register 20 held. The flash memory address selector 50 chooses the address of an address bus 1, and the address which the memory control means 11 outputs. A flash memory 51 considers the address which the flash memory address selector 50 outputs as an address input. The flash memory data buffer 52 connects a flash memory 51 and a data bus 2. The data memory address selector 41 chooses the part II part address of the addresses of an address bus 1, and the address for the control which the memory control means 11 outputs. A data flag is set corresponding to the address with which data memory 42 has the memory capacity of the same magnitude as the block which is the unit which performs writing and elimination of a flash memory 51, and considers the address which the data memory address selector 41 outputs as an address input, and data are written in. The data memory data buffer 43 connects data memory 42 and a data bus 2.

[0024] The memory control means 12 makes a comparator 30 compare the address of an address bus 1, and the address held at the address register 20 here at the time of data read-out. When an inequality output occurs from a comparator 30, the data by which were made to supply the address of an address bus 1 to a flash memory 51 through the flash memory address selector 50, and were made to carry out reading appearance of the data of the address of an address bus 1 from a flash memory 51, and reading appearance was carried out from the flash memory 51 are sent out to a data bus 2 through the flash memory data buffer 52.

[0025] moreover, when a coincidence output occurs from a comparator 30 The part II part address of the addresses of an address bus 1 is supplied to data memory 42 through

the data memory address selector 41. When the data flag corresponding to the part II part address of the addresses of an address bus 1 is set to data memory 42, reading appearance of the data of the part II part address of the addresses of an address bus 1 is carried out from data memory 42. The data by which reading appearance was carried out are sent out from data memory 42 to a data bus 2 through the data memory data buffer 43. When the data flag corresponding to the part II part address of the addresses of an address bus 1 is not set to data memory 42, the address of an address bus 1 is made to supply to a flash memory 51 through the flash memory address selector 50. The data by which were made to carry out reading appearance of the data of the address of an address bus 1 from a flash memory 51, and reading appearance was carried out from the flash memory 51 are sent out to a data bus 2 through the flash memory data buffer 52.

[0026] moreover, while the memory control means 11 is not writing in data once [after / powering on] at the time of data writing The part I part address of the addresses of an address bus 1 is made to write in an address register 20. By giving the part II part address of the addresses of an address bus 1 to data memory 42 through the data memory address selector 41 While making the location corresponding to the part II part address of the addresses of the address bus 1 of data memory 42 memorize the data of a data bus 1 through the data memory data buffer 43 The data flag corresponding to the part II part address of the addresses of an address bus 1 is made to set.

[0027] Moreover, the memory control means 11 makes a comparator 30 compare the part I part address and the part I part address of an address bus 1 which the address register 20 held, while writing in data once at least after powering on at the time of data writing. In this case, when a coincidence output occurs from a comparator 30 By giving the part II part address of the addresses of an address bus 1 to data memory 42 through the data memory address selector 41 While making the location corresponding to the part II part address of the addresses of the address bus 1 of data memory 42 memorize the data of a data bus 2 through the data memory data buffer 43 The data flag corresponding to the part II part address of the addresses of an address bus 1 is made to set.

[0028] Moreover, when an inequality output occurs from a comparator 30 It lets the data memory address selector 41 and the flash memory address selector 50 pass for each address included in the block corresponding to the part I part address which the address register 20 held [sequential], respectively. By giving in common to data memory 42 and a flash memory 51 Data are made to copy to data memory 42 only about the address with which the data flag is not set by data memory 42 among each address included in the block corresponding to the part I part address of the addresses of the

address bus in a flash memory 51. The data of the block corresponding to the part I part address of the addresses of the address bus 1 in a flash memory 51 are eliminated. The data of data memory 42 are made to write in the block corresponding to the part I part address of the addresses of the address bus 1 in a flash memory 51. Cancel the set of the data flag of data memory 42, and the part I part address of the addresses of an address bus 1 is made to write in an address register 20. By giving the part II part address of the addresses of an address bus 1 to data memory 42 through the data memory address selector 41 While making the location corresponding to the part II part address of the addresses of the address bus 1 of data memory 42 memorize the data of a data bus 2 through the data memory data buffer 43 He is trying to make the data flag corresponding to the part II part address of the addresses of the address bus 1 of data memory 42 set.

[0029] Hereafter, actuation of flash memory equipment is explained in detail. When data are not once written to flash memory equipment yet after powering on, the part I part address of the block numbers of the address which had writing first, i.e., the address of an address bus 1, is written in an address register 20. data are written in the address corresponding to the part II part address of the addresses of an address bus 1, and the data flag section 61 is set to it, simultaneously the data division 60 of data memory 42. At this event, write-in actuation is not performed to a flash memory 51.

[0030] Actuation of the gestalt of this operation is divided and explained to read-out and writing, referring to drawing 2 . First, read-out is explained. Read-out has two conditions. In the address register 20, the block number with which writing was in the past is held. Only the reading appearance from the block with which only the reading appearance from the block with which two conditions wrote in in the past was writing in in the past is determined.

[0031] In read-out from the block which had not written in in the past, the inequality signal which shows the inequality of the address from a comparator 30 is outputted. In this case, the address of an address bus 1 is added to a flash memory 51 through the flash memory address selector 50 at the time of read-out. A flash memory 51 outputs the data of the added address, and outputs data to a data bus 2 through the flash memory data buffer 52. The memory control means 11 controls the selection direction of the flash memory address selector 50, and the flash memory data buffer 52. In this case, it becomes simple memory read-out.

[0032] When reading from the block which wrote in, the coincidence signal which shows that it was in agreement from the comparator 30 is outputted. In this case, the address of an address bus 1 is added to data memory 42 through the data memory address selector 41. If the signal which shows that there was writing is acquired from the data

flag section 61 (drawing 4) of data memory 42, the output of the data division 60 of data memory 42 will be outputted to a data bus 2 through the data memory data buffer 43. That is, the data written to data memory 42 in the past will be read from data memory 42. if the signal which shows that there was no writing is acquired from the data flag section 61 (drawing 4) of data memory 42 -- the address of an address bus 1 -- the flash memory address selector 50 -- a passage -- a flash memory 51 -- adding -- having . A flash memory 51 outputs the data of the added address, and outputs data to a data bus 2 through the flash memory data buffer 52. In this case, it means reading data from a flash memory 51.

[0033] Below, the writing of data is explained. Writing can roughly be decomposed into three actuation. The 1st is the case where data are not once written to flash memory equipment yet after powering on. In the case where the writing to the same block as the block written in recently is performed, the 2nd is the case where the 3rd performs the writing to the block written in recently and the different block.

[0034] When the writing to the same block as the block written in recently is performed and the address given from an address bus 1 and the content of the address register 20 are compared by the comparator 30, from a comparator 30, the coincidence signal which shows that it was in agreement is outputted, this is given to the memory control means 11, and the control approach is determined. Others are the same as the case where data are not once written to flash memory equipment yet after powering on who explained previously.

[0035] When the writing to the block written in recently and the different block is performed and the content of the address given from an address bus 1 and the address register 20 is compared by the comparator 30, from a comparator 30, the inequality signal which shows that it is not in agreement is outputted, this is given to the memory control means 11, and the control approach is determined. In this case, it writes in to a flash memory 51. Write-in actuation is decomposed into five phases.

[0036] The 1st copies the content of the flash memory 51 to data memory 42. The memory control means 11 performs the following actuation, making a sequential change of the address to a flash memory 51 and data memory 42. If data memory 42 is read first and the data flag section 61 is set, since it is shown that writing has taken place, it advances to the next address. if the data flag section 61 is not set, the data which carried out reading appearance of the flash memory 51, and carried out reading appearance to the data division 60 of data memory 42 are written in. The data which should update a flash memory 51 are able to be prepared for data memory 42 above.

[0037] It is writing of as opposed to [as opposed to / in the 2nd phase / elimination of a flash memory 51] a flash memory 51 in the 3rd phase, and this is the same as the 3rd

step explained with the gestalt of the 1st operation, and the 4th step. The 4th phase is elimination of the data flag section 61 of data memory 42. The memory control means 11 writes in the condition that data are not set to the data flag section 61 of data memory 42.

[0038] The 5th phase is written in to an address register 20 and data memory 42, and holds information. The block number of the address with writing is written in an address register 20. Data are written in data memory 42 to the address corresponding to it and coincidence at data division 60, and the data flag section 61 is set. In addition, since access is kept waiting with the control signal output 4 while performing the writing to a flash memory 51 unlike the gestalt of the 1st operation, while writing in the flash memory 51, the demand of read-out or writing does not come.

[0039] As mentioned above, since according to the gestalt of this operation an address register 20, a comparator 30, the data memory address selector 41, data memory 42, the data memory data buffer 43, and the flash memory address selector 51 are formed and the writing to a flash memory 51 was controlled by the memory control means 11, complicated memory write-in actuation to a flash memory 51 can be performed easily, without needing the software of dedication, and treating like the usual memory is possible. Therefore, it can access without being conscious of a flash memory 51, and the software created for the memory of the general result can be worked as it is. In addition, in the continuous writing to the same block, the writing to a flash memory 51 does not take place, but it completes in writing once to the continuous writing of as opposed to [since it writes in and comes out and writing takes place for the first time] the same block to another block, therefore it writes in and a count can be lessened, it decreases and the access-restriction time amount by writing can do comparatively few in the degradation by using a flash memory 51.

[0040] In addition, if an address register and 1 set of data register are added, it can avoid keeping a bus waiting also to the writing from the bus by which the writing to a flash memory 51 takes place like the gestalt of the 1st operation. Moreover, the data memory address selector 41, data memory 42, and the data memory data buffer 43 can be replaced by the dual port memory 45 which has two data terminals DT1 and DT2 corresponding to two address terminals AD1 and AD2 as shown in drawing 6 , and these address terminals AD1 and AD2, respectively. Specifically two input terminals of the data memory address selector 41 and two address terminals AD1 and AD2 of dual port memory 45 correspond, the output terminal of data memory 42 and one data terminal DT 1 of dual port memory 45 correspond, and the output terminal of the data memory data buffer 43 and the data terminal DT 2 of another side of dual port memory 45 correspond.

[0041] (Gestalt of the 3rd operation) Drawing 3 is the block diagram showing the configuration of the flash memory equipment in the gestalt of operation of the 3rd of this invention. drawing 3 -- setting -- 1 -- an address bus and 2 -- a data bus and 3 -- a control signal input and 4 -- a control signal output and 12 -- a memory control means and 21 -- an address tag memory address selector and 22 -- address tag memory and 23 -- an address tag memory data buffer and 30 -- for data memory and 43, as for a flash memory address selector and 51, a data memory data buffer and 50 are [a comparator and 41 / a data memory address selector and 42 / a flash memory and 52] flash memory data buffers.

[0042] Drawing 5 (a) shows the bit pattern of the address of flash memory equipment, and drawing 5 (b) shows the bit pattern of the address tag memory 22. In the bit pattern of the address of the flash memory equipment of drawing 5 (a), the left-hand side of drawing shows the high-order-digit side. Being able to divide the whole into three parts (the part I part address (for example, upper address), the part II part address (for example, middle address), the part III part address (for example, lower address)), a low-ranking digit (the part III part address) is a part equivalent to the block-address space of a flash memory 51. For example, if the magnitude of a block is the 256 addresses, 8 bits corresponds to this. The following part (the part II part address) is a part added to the address of the address tag memory 22. This part and the part equivalent to the block address like the point are added to the address of data memory 42. The part (the part I part address) in which the address remains is added to the data of the address tag memory 22.

[0043] In the bit pattern of the data of the address tag memory 22 of drawing 5 (b), the top section (the part I part address) of drawing 5 (a) was added to data (a part of block number of the data stored in data memory 42), and 62 is written in according to the conditions which are an event of writing in to the address tag section, a call, and a flash memory 51. As for this part, the memory control means 12 can perform read-out and writing, and read-out from an address bus 1 and a data bus 2 and writing are not made. 63 is the address tag flag section, it is written in according to the conditions which are an event of writing in to a flash memory 51, and it is shown that the address tag section 62 is effective, and if writing takes place to the address tag section 62, it will be set. this part can be written in by the memory control means 12 carrying out reading appearance, and carries out reading appearance from an address bus 1 and a data bus 2, and writing is not made.

[0044] Below, flash memory equipment is explained. This flash memory equipment performs writing and elimination for the block which consists of two or more memory cells as a unit. In this, the memory control means 12 controls the whole. The address tag

memory address selector 21 chooses the part II part address corresponding to the block number of the block which should perform writing and elimination of the addresses which consist of the part I part address, the part II part address, and the part III part address of an address bus 1, and the address which the memory control means 12 outputs. An address tag flag is set corresponding to the address with which the address tag memory 22 considers the address outputted from the address tag memory address selector 21 as an address input, and data are written in. The address tag memory data buffer 23 connects the address tag memory 22 and an address bus 1, and supplies the part I part address of an address bus 1 to the address tag memory 22 as a data input. A comparator 30 compares with the part I part address of the addresses of an address bus 1 the address by which reading appearance is carried out from the address tag memory 22 by considering the part II part address of the addresses of an address bus 1 as an address input. The flash memory address selector 50 chooses the address of an address bus 1, and the address which the memory control means 12 outputs. A flash memory 51 considers the address outputted from the flash memory address selector 50 as an address input. The flash memory data buffer 52 connects a flash memory 51 and a data bus 2. The data memory address selector 41 chooses the part II part address of the addresses of an address bus 1 and the part III part address, and the address for the control which the memory control means 12 outputs. A data flag is set corresponding to the address with which data memory 42 has the same capacity as a part for the number equivalent to the magnitude of the address space of the part II part address of the block which is the unit of the writing and elimination of a flash memory 51, and considers the address which the data memory address selector 41 outputs as an address input, and data are written in. The data memory data buffer 43 connects data memory 42 and a data bus 2.

[0045] The above-mentioned memory control means 12 makes a comparator 30 compare the data to which reading appearance of the address tag memory address selector 21 was carried out for the part II part address of the part I part address of the addresses of an address bus 1, and the addresses of an address bus 1 from the address tag memory 22 as a through address input at the time of data read-out. In this case, when an inequality output occurs from a comparator 30, the data by which were made to supply the address of an address bus 1 to a flash memory 51 through the flash memory address selector 50, and were made to carry out reading appearance of the data of the address of an address bus 1 from a flash memory 51, and reading appearance was carried out from the flash memory 51 are sent out to a data bus 2 through the flash memory data buffer 52.

[0046] moreover, when a coincidence output occurs from a comparator 30 The part II

part address of the addresses of an address bus 1 and the part III part address are supplied to data memory 42 through the data memory address selector 41. When the data flag corresponding to the part II part address of the addresses of an address bus 1 and the part III part address is set to data memory 42 being alike -- the data by which were made to carry out reading appearance of the data of the part II part address of the addresses of an address bus 1 and the part III part address from data memory 42, and reading appearance was carried out from data memory 42 are sent out to a data bus 2 through the data memory data buffer 43. The data by which were made to supply the address of an address bus 1 to a flash memory 51 through the flash memory address selector 50 on the other hand when the data flag corresponding to the part II part address of the addresses of an address bus 1 and the part III part address was not set to data memory 42, and were made to carry out reading appearance of the data of the address of an address bus 1 from a flash memory 51, and reading appearance was carried out from the flash memory 51 are sent out to a data bus 2 through the flash memory data buffer 52.

[0047] moreover, before the memory control means 12 completes the writing to all the addresses of the address tag memory 22 at the time of data writing While considering the address tag memory address selector 21 for the part II part address of the addresses of an address bus 1 as a through address input and making it write in the address tag memory 22 by making the part I part address of the addresses of an address bus 1 into a data input The address tag flag corresponding to the address which performed the data writing in the address tag memory 22 is made to set. By giving the part II part address of the addresses of an address bus 1, and the part III part address to data memory 42 through the data memory address selector 41 While making the location corresponding to the part II part address of the addresses of the address bus 1 of data memory 42, and the part III part address memorize the data of a data bus 2 through the data memory data buffer 43 The data flag corresponding to the part II part address of the addresses of the address bus 1 in data memory 42 and the part III part address is made to set.

[0048] furthermore, after the writing to all the addresses of the address tag memory 22 is completed and all the address tag flags of all of the address tag memory 22 that carried out the address mapping are set at the time of data writing, the memory control means 12 A comparator 30 is made to compare the data which carried out reading appearance from the address tag memory 22 by considering the part II part address of the part I part address of the addresses of an address bus 1, and the addresses of an address bus 1 as an address input.

[0049] in this case, when a coincidence output occurs from a comparator 30 By giving the part II part address of the addresses of an address bus 1, and the part III part

address to data memory 42 through the data memory address selector 41 While making the location corresponding to the part II part address of the addresses of the address bus 1 of data memory 42, and the part III part address memorize the data of a data bus 2 through the data memory data buffer 43 The data flag corresponding to the part II part address of the addresses of the address bus 1 of data memory 42 and the part III part address is made to set.

[0050] moreover, when an inequality output occurs from a comparator 30 With the data which all the addresses and those addresses of the address tag memory 22 were made to memorize It lets the data memory address selector 41 and the flash memory address selector 50 pass for each address included in the block of the number corresponding to two or more sets of part I part addresses and the part II part address which are decided, respectively [sequential], respectively. By giving in common to data memory 42 and a flash memory 51 Only about the address with which the data flag is not set by data memory 42 among each address included in the block of the number corresponding to two or more sets of part I part addresses in the address of the address bus 1 in a flash memory 51, and the part II part address, data It is made to copy to data memory 42. It continues and the data of the block corresponding to two or more sets of part I part addresses and the part II part address which are decided, respectively with the data which all the addresses and those addresses of the address tag memory 22 were made to memorize are eliminated. It continues and the data of data memory 42 are made to write in the block corresponding to two or more sets of part I part addresses in the address of the address bus 1 in a flash memory 51, and the part II part address. It continues and the set of the data flag of data memory 42 is canceled. While making it write in the address tag memory 22 by making the part I part address of the addresses of an address bus 1 into a data input while considering the address tag memory address selector 21 for the part II part address of the addresses of an address bus 1 as a through address input until it completes the writing to all the addresses of the address tag memory 22 continuously, the address tag flag corresponding to the address which performed the data writing in the address tag memory 22 is made to set. Moreover, by giving the part II part address of the addresses of an address bus 1, and the part III part address to data memory 42 through the data memory address selector 41 While making the location corresponding to the part II part address of the addresses of the address bus 1 of data memory 42, and the part III part address memorize the data of a data bus 2 through the data memory data buffer 43 The data flag corresponding to the part II part address of the addresses of the address bus 1 in data memory 42 and the part III part address is made to set.

[0051] Since the fundamental actuation in the gestalt of this operation is close to the

gestalt of the 2nd operation, only a part with that difference is explained in more detail. A big difference is replaced with an address register 20, and is the increase of capacity and the point carried out of data memory 42 corresponding to the address tag memory address selector 21, the address tag memory 22, the point using the address tag memory data buffer 23, and its capacity. Thereby, to two or more blocks, the written-in data can be held and the writing to a flash memory 51 can be reduced more compared with the gestalt of the 2nd operation.

[0052] In read-out, the block which wrote in in the past is recorded on the address tag memory 22. At the time of read-out to the block from which writing had not taken place in the past, a comparator 30 emits an inequality signal, this is received, and the memory control means 12 makes the path of an address bus 1, the flash memory address selector 50, a flash memory 51, the flash memory data buffer 52, and a data bus 2. This becomes direct read-out from a flash memory 51.

[0053] At the time of read-out to the block from which writing took place in the past, a comparator 30 emits a coincidence signal, this is received, and, as for the memory control means 12, two paths, the path of an address bus 1, the data memory address selector 41, and data memory 42 and the path of an address bus 1, the flash memory address selector 50, and a flash memory 51, in all are made first. Here, if the signal which shows that the past had writing is acquired from the data flag section 61 of data memory 42, the path of the data memory data buffer 43 and a data bus 2 will be made, and the content which wrote in the past will be outputted. On the other hand, if the signal which shows that there was no writing in the past is acquired from the data flag section 61 of data memory 42, the path of the flash memory data buffer 52 and a data bus 2 will be made, and the content of the flash memory 51 will be outputted.

[0054] If the signal which shows in writing that it was in agreement from the comparator 30 is acquired, since it will be the block which wrote in in the past, the data memory address selector 41 and the content written in in the path of data memory 42 are stored in data memory 42. If the signal which shows an inequality is acquired from a comparator 30, the writing to a flash memory 51 will be performed. This part is the same as the gestalt of the 2nd operation. If the writing to a flash memory 51 is completed, renewal of the address tag memory 22 and data memory 42 will be performed.

[0055] According to the gestalt of this operation, as mentioned above The address tag memory address selector 21, the address tag memory 22, the address tag memory data buffer 23, a comparator 30, the data memory address selector 41, data memory 42, the data memory data buffer 43, and the flash memory address selector 51 Since it prepares and the writing to a flash memory 51 was controlled by the memory control means 12

Complicated memory write-in actuation to a flash memory 51 can be performed easily, without needing the software of dedication, and treating like the usual memory is possible. Therefore, it can access without being conscious of a flash memory 51, and the software created for the memory of the general result can be worked as it is. In addition, by the continuous writing to two or more blocks, the writing to a flash memory 51 does not take place, but it completes in writing once to the continuous writing of as opposed to [since it writes in and comes out and the writing of two or more blocks takes place for the first time] two or more blocks to another blocks other than two or more above-mentioned blocks, and write-in time amount can be shortened further. Therefore, the count of writing can be lessened further, and the access-restriction time amount by writing decreases further, and can lessen degradation by using a flash memory 51 further.

[0056] In addition, it can replace with the address tag memory address selector 21, the address tag memory 22, and the address tag memory data buffer 23, and the dual port RAM 24 which has two data terminals DT1 and DT2 corresponding to two address terminals AD1 and AD2 as shown in drawing 7 , and these address terminals AD1 and AD2 can also be used. Two input terminals of the address tag memory address selector 21 and two address terminals AD1 and AD2 of a dual port RAM 24 correspond, and, specifically, it corresponds with the output terminal of the address tag memory 22, and one data terminal DT 1 of a dual port RAM 24. In addition The data terminal DT 2 of another side of a dual port RAM 24 is connected to address terminal AD2 of a dual port RAM 24.

[0057] Moreover, it is possible to rearrange the location sequence of the bit pattern of an address space into drawing 5 (a), and there is also no need of dividing a bit continuously. As the gestalt of the 2nd operation described, it is also possible by placing an address register and a data register before an address memory address selector and a data memory address selector to open a bus in early stages of write-in actuation.

[0058]

[Effect of the Invention] According to flash memory equipment according to claim 1, since the writing to a flash memory was controlled by the memory control means, complicated memory write-in actuation to a flash memory can be performed easily, without needing the software of dedication, and treating like the usual memory is possible. therefore, the degradation by the old personal computer which used general memory, and the software of a Personal Digital Assistant being able to use as it is, and in addition using a flash memory -- few -- it can do -- in addition -- and a memory apparatus without the danger by a cell being lost can be realized, and it is dramatically advantageous practically.

[0059] According to flash memory equipment according to claim 2, since the writing to a flash memory was controlled by the memory control means, complicated memory write-in actuation to a flash memory can be performed easily, without needing the software of dedication, and treating like the usual memory is possible. And it completes in writing once to the continuous writing to the same block, and write-in time amount can be shortened. therefore, the degradation by the old personal computer which used general memory, and the software of a Personal Digital Assistant being able to use as it is, and in addition using a flash memory -- few -- it can do -- in addition -- and a memory apparatus without the danger by a cell being lost can be realized, and it is dramatically advantageous practically. According to flash memory equipment according to claim 3, since the writing to a flash memory was controlled by the memory control means, complicated memory write-in actuation to a flash memory can be performed easily, without needing the software of dedication, and treating like the usual memory is possible. And it completes in writing once to the continuous writing to two or more blocks, and write-in time amount can be shortened further. therefore, the degradation by the old personal computer which used general memory, and the software of a Personal Digital Assistant being able to use as it is, and in addition using a flash memory -- few -- it can do -- in addition -- and a memory apparatus without the danger by a cell being lost can be realized, and it is dramatically advantageous practically.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the configuration of the flash memory equipment in the gestalt of operation of the 1st of this invention.

[Drawing 2] It is the block diagram showing the configuration of the flash memory equipment in the gestalt of operation of the 2nd of this invention.

[Drawing 3] It is the block diagram showing the configuration of the flash memory equipment in the gestalt of operation of the 3rd of this invention.

[Drawing 4] It is the schematic diagram showing the bit pattern of the data of data memory.

[Drawing 5] It is the outline schematic drawing showing the bit pattern of the data of address tag memory.

[Drawing 6] It is a schematic diagram for explaining the replacement to dual port

memory from a data memory address selector, data memory, and a data memory data buffer.

[Drawing 7] It is a schematic diagram for explaining the replacement to an address tag memory address selector, address tag memory, and dual port memory from an address tag memory data buffer.

[Description of Notations]

1 Address Bus

2 Data Bus

3 Control Signal Input

4 Control Signal Output

10 Memory Control Means

11 Memory Control Means

12 Memory Control Means

20 Address Register

21 Address Tag Memory Address Selector

22 Address Tag Memory

23 Address Tag Memory Data Buffer

30 Comparator

40 Data Register

41 Data Memory Address Selector

42 Data Memory

43 Data Memory Data Buffer

44 Data Memory

50 Flash Memory Address Selector

51 Flash Memory

52 Flash Memory Data Buffer

60 Data Division

61 Data Flag Section

62 Address Tag Section

63 Address Tag Flag Section

[Translation done.]

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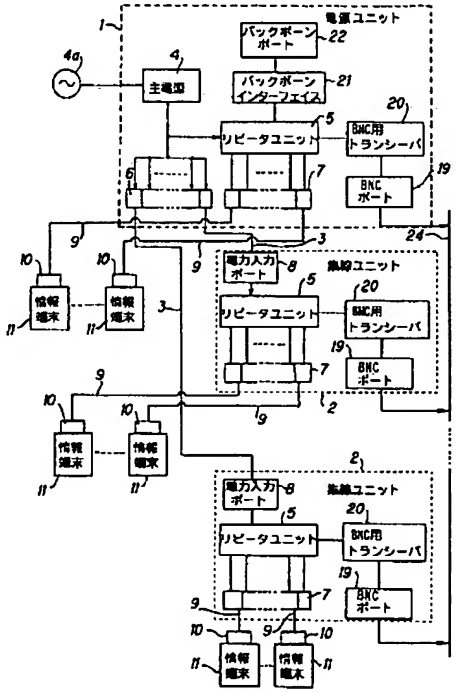
(54)【発明の名称】　集線装置

(57)【要約】

【課題】　集線ユニットの移動や設置位置に制限があり、安全性および汎用性が低く、大型化およびコスト高を招く。

【解決手段】　複数の集線ユニット２に共通した電源ユニット１を有する。電源ユニット１は外部の商用電源４ａよりＡＣ電力を入力し、所定の電圧のＤＣ電力を出力する。電源ユニット１と複数の集線ユニット２はツイストペア線９とは独立した配電線３によって接続される。



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【特許請求の範囲】

【請求項１】外部電源に接続されて所定の電圧の電力を出力する電源ユニットと、前記電力を配電線を介して受け、第１の情報端末からツイストペア線を介して入力した信号を再生して第２の情報端末へ前記ツイストペア線を介して出力する集線ユニットを備え、

前記電源ユニットは、前記外部電源に接続されて前記所定の電圧の電力を発生する主電源部と、前記所定の電圧の電力を出力する電力出力ポートを有し、

前記集線ユニットは、前記所定の電圧の電力を前記配電線を介して入力する電力入力ポートと、前記所定の電圧の電力に基づいて前記信号を再生するリピータユニットと、前記信号を前記第１の情報端末から前記ツイストペア線を介して入力し、再生された前記信号を前記ツイストペア線を介して前記第２の情報端末へ出力するツイストペアポートを有することを特徴とする集線装置。

【請求項２】前記電源ユニットは、前記所定の電圧の電力に基づいて第３の情報端末の信号を再生するリピータユニットと、前記第３の情報端末から前記信号をツイストペア線を介して入力し、再生された前記信号を前記ツイストペア線を介して第４の情報端末へ出力するツイストペアポートを有す構成の請求項１記載の集線装置。

【請求項３】前記電源ユニットは、前記配電線を介して複数の前記集線ユニットに接続され、

前記複数の前記集線ユニットは、前記ツイスト線を介してそれぞれ対応する２つ以上の情報端末と接続されている構成の請求項１記載の集線ユニット。

【請求項４】前記電源ユニットおよび前記集線ユニットは、それぞれの前記リピータユニットがトランシーバ手段を介して接続されている構成の請求項２記載の集線装置。

【発明の詳細な説明】

【０００１】

【発明が属する技術分野】本発明は、ツイストペア線を伝送媒体としてＩＥＥＥ８０２．３規格によるＣＳＭＡ／ＣＤ（搬送波感知多重アクセス／衝突検出）方式を用いたローカルエリアネットワーク（以下、「ＬＡＮ」という）に使用される集線装置に関し、特に、システムのフレキシビリティを向上させて、容易に集中配置または分散配置を可能にした集線装置に関する。

【０００２】

【従来の技術】従来、複数のコンピュータ（以下、「情報端末」という）をネットワークで接続した分散処理システムとして、ＩＥＥＥ８０２．３規格に代表されるＣＳＭＡ／ＣＤ方式のＬＡＮが知られている。特に、配線の容易性から１０ＢＡＳＥ－Ｔ規格に準拠したツイストペア線を伝送媒体としたものが広く普及している。ツイストペア線を用いてＬＡＮを構築する場合には、ＨＵＢ（ハブ）、マルチポートリピータとも言われる集線ユニットを中心にして、各情報端末をツイストペア線でスター状に接続する構成が一般的である。その具体的構成例を図２および図３に示す。

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【０００３】図２において、集線ユニット２は、ＴＰ－ＭＡＵ（Twisted Pair-Media Attachment Unit）１０を有するパソコン、ワークステーション、サーバ等の情報端末１１とツイストペア線９によって接続されている。この集線ユニット２はツイストペア線９に接続されるツイストペアポート７と、リピータ機能を実行するリピータユニット５と、外部の商用電源１５ａと給電線１３を介して接続された電源入力部１４と、電源入力部１４からＡＣ電圧を受けて５Ｖおよび１２ＶのＤＣ電力をリピータユニット５へ出力する電源部１５を有する。

【０００４】以上の構成において、情報端末１１の信号はＴＰ－ＭＡＵ１０によって変換された後ツイストペア線９に出力される。ツイストペア線９により伝送された信号は、ツイストベアポート７よりリピータユニット５に入力される。リピータユニット５は、入力された信号を再生して、入力したポート以外のツイストペアポート７より出力する。

【０００５】図３において、図２と同一の部分には同一の引用数字を付したので重複する説明は省略するが、ＡＤ／ＤＣ変換回路１６は外部の商用電源１５ａより給電線１３を介してＡＣ電圧を入力し、これをＤＣ電圧にして集線ユニット２の電源入力部１７へ出力する。集線ユニット２では、定電圧回路１８が電源入力部１７から入力するＤＣ電圧を５Ｖおよび１２ＶのＤＣ定電圧にしてリピータユニット５へ出力する。

【０００６】以上から明らかなように、集線ユニットの近傍に外部電源があり、かつ集線ユニットが１台の場合は、ツイストペア線を配線するだけで、手軽にシステムの構築が可能になり、かつ、使い勝手がよいシステムが得られる。また、従来のＬＡＮへの電力供給システムとして、例えば、特開平６－１９７４３３号（特願平４－３４２９３４号）に示される電力配線統合ＨＵＢがある。

【０００７】この電力配線統合ＨＵＢは、ポート数を限定して小型化することにより、ＩＥＥＥ８０２．３規格に準拠するＬＡＮのマルチポートリピータを床下に収納することを可能とし、情報配線システムを床下電力配線システムに統合できるようにしており、その構成は電源入力部と、カスケード接続部と、マルチポートリピータ部を有し、電源入力部に床下電力配線システムのジョイントボックスと嵌合するコネクタを設け、カスケード接続部にネットワークと接続する手段を設けている。そのため、情報配線システムと床下電力配線システムとの統合が可能になり、すでに床下電力配線システムがある場所においては、フロアの美観を損なわず、ネットワーク管理を容易にし、フレキシブルなレイアウト変更を可能にしている。

【０００８】更に、従来の集線装置として、例えば、特

開平６－５３９７０号（特願平４－２０１６３１号）に示されるものがある。この集線装置は、情報端末の電源からリピータユニットに電力を供給することにより外部電源を不要にしており、その構成はＴＰ－ＭＡＵと集線ユニットを有し、ＴＰ－ＭＡＵは情報端末から供給される電力をツイストペア線に出力する定電圧回路等を有し、集線ユニットの内部に共通バスを設けてリピータ回路をツイストペア線毎に独立させ、各ツイストペア線から供給される電力でそのツイストペア線に接続されたリピータ回路を動作させるようにしている。そのため、外部電源が不要になり、ツイストペア線を用いたＬＡＮの設計時やレイアウト変更時にも、電源配線を必要とせず、設置や移動を容易に行う事ができる。

【０００９】

【発明が解決しようとする課題】しかし、図２および図３に示した集線装置によると、接続される情報端末が多くなって複数台の集線ユニットが必要になると、各集線ユニット毎に外部電源から電力を供給しなければならないので、集線ユニットがＬＡＮシステムの構築時やレイアウト変更時に移動や設置の位置で制限を受ける。特に、複数の集線ユニットを同一の場所に設置する場合には、複数の給電線やＡＣ／ＤＣ変換回路が外部電源に接続されるため、作業者、使用者、設備等において安全性に問題がある。

【００１０】また、特開平６－１９７４３３号に示された電力統合ＨＵＢによると、床下電力配線システムのジョイントボックスと嵌合する専用のコネクタが必要になるので、汎用性が低下する。また、情報配線システムの構築においても、既に床下電力配線システムが構築されている場合は、それを考慮しなければならず、また、新たに構築する場合は、情報配線システムと合せて床下電力配線システムの構築を行わなければならないので、システム構築に制限を受けることになる。

【００１１】更に、特開平６－５３９７０号に示された集線装置によると、ツイストペア線毎にリピータ回路及び定電圧回路が必要なため、構成部品点数が増加して大型化およびコスト高になる。また、ＴＰ－ＭＡＵ毎に電力を供給するための定電圧回路および電源ラインを設け、集線ユニットにリピータ回路毎に定電圧回路を設けているので、ＩＥＥＥ８０２．３規格の一般的な製品の使用が出来ず、汎用性が低下する。更に、断線し易いツイストペア線により電源を供給するので、安全性において問題がある。

【００１２】従って、本発明の目的は集線ユニットの移動や設置の位置で制限を受けない集線装置を提供することにある。本発明の他の目的は作業者、使用者、設備等において安全性の高い集線装置を提供することにある。本発明の他の目的は汎用性が高く、大型化およびコスト高が抑えられる集線装置を提供することにある。

【００１３】

【課題を解決するための手段】本発明は、上記の目的を実現するため、外部電源に接続されて所定の電圧の電力を出力する電源ユニットと、前記電力を配電線を介して受け、第１の情報端末からツイストペア線を介して入力した信号を再生して第２の情報端末へ前記ツイストペア線を介して出力する集線ユニットを備え、前記電源ユニットは、前記外部電源に接続されて前記所定の電圧の電力を発生する主電源部と、前記所定の電圧の電力を出力する電力出力ポートを有し、前記集線ユニットは、前記所定の電圧の電力を前記配電線を介して入力する電力入力ポートと、前記所定の電圧の電力に基づいて前記信号を再生するリピータユニットと、前記信号を前記第１の情報端末から前記ツイストペア線を介して入力し、再生された前記信号を前記ツイストペア線を介して前記第２の情報端末へ出力するツイストペアポートを有することを特徴とする集線装置を提供する。

【００１４】

【発明の実施の形態】以下、本発明の第１の実施の形態における集線装置を図１に基づいて説明する。図１において、１は外部電源（商用電源）４ａからのＡＣ電力の供給を受け、ＤＣ５Ｖおよび１２ＶのＤＣ電力に変換して出力する電源ユニットである。２は電源ユニット１からＤＣ電力の供給を受けて動作する集線ユニット、３は電源ユニット１から出力されたＤＣ電力を集線ユニット２へ給電するための配電線である。

【００１５】電源ユニット１は、外部電源４ａの１００ＶのＡＣ電力から５Ｖおよび１２ＶのＤＣ電力を発生する主電源部４と、集線ユニット２へ電力を出力する複数の電力出力ポート６と、入力した信号を再生して出力するリピータユニット５と、リピータユニット５へ信号を入出力するツイストペアポート７と、集線ユニット２との間で情報伝送を行うＢＮＣ用トランシーバ２０と、ＢＮＣ用トランシーバ２０へ信号を入出力するＢＮＣポート１９とを有しており、ＢＮＣポート１９は、例えば、同軸ケーブルの伝送ライン２４に結合されている。更に、バックボーン回線（ＩＥＥＥ８０２．３の１０ＢＡＳＥ－Ｔ規格に準拠した同軸回線、ＦＤＤＩ回線、高速ＬＡＮ回線、等に接続できるように、バックボーンポート２２及びバックボーンインターフェース回路２１を有している。

【００１６】集線ユニット２は、電源の入力部である電力入力ポート８と集線機能を有するリピータユニット５と、ツイストペアポート７を有し、更に電源ユニット１および集線ユニット２の間で情報伝送を行うために、リピータユニット５と接続されたＢＮＣ用トランシーバ２０と、ＢＮＣポート１９とを有している。配電線３は、集線ユニット２に対する給電線であり、電源ユニット１の電力出力ポート６および集線ユニット２の電力入力ポート８と嵌合するコネクタ（図示せず）を両端に有する。そのコネクタは、ロック機能を有し、電力出力ポー

ト6および電力入力ポート8と嵌合した場合、不注意等によって外れない構造となっている。

【0017】パソコン、ワークステーション、サーバ、等の情報端末11はTP-MAU10を介してツイストペア線9によって集線ユニット2のツイストペアポート7に接続されており、そこから出力された信号はTP-MAU10においてツイストペア線9上に伝送可能な信号に変換された後、ツイストペア線9に出力される。ツイストペア線9により伝送された信号は、ツイストペアポート7よりリピータユニット5に入力される。リピータユニット5は、入力された信号を再生して入力したポート以外のツイストペアポート7より出力する。

【0018】リピータユニット5を動作させるための電源は、電源ユニット1の主電源部4（AC-DC電源、スイッチング電源、等と呼ばれている）に統合されている。主電源部4は、外部電源4aの電源電圧（AC100V）をリピータユニット5の動作可能な電圧（DC5V，12Vなど）に変換し、主電源部4より出力されたDC電力を内部配線にて複数に分岐して内部のリピータユニット5に供給し、かつ、電力出力ポート6より集線ユニット2のリピータユニット5が動作できるようにDC電力を出力する。

【0019】電力出力ポート6より出力されたDC電力は、配電線3を伝送媒体として集線ユニット2の電力入力ポート8に入力し、このDC電力によりユニット2のリピータユニット5を駆動する。電源ユニット1の電力出力ポート6および集線ユニット2の電力入力ポート8は、それぞれ配電線2と嵌合した場合、不注意によって配電線2が外れないコネクタの構造を有する。

【0020】前述したように、電源ユニット1および集線ユニット2は、IEEE802．3の10BASE2規格に準拠したBNCポート19を有し、電源ユニット1と集線ユニット2、および集線ユニット2の相互の間の情報の伝送を、例えば、同軸回線の伝送ライン24を用いて実現している。また、電源ユニット1のリピータユニット5はバックボーンインターフェース回路21およびバックボーンポート22のコネクタを内蔵しており、バックボーン回線であるIEEE802．3の10

BASE5規格に準拠した同軸回線や高速LAN、等の回線に接続することができる。これによってLANを構築することができる。

【0021】

【発明の効果】以上説明した通り、本発明の集線装置によると、集線ユニットの電源を電源ユニットに統合して配電線により分電するので、複数の集線ユニットを1箇所に集中設置する場合においても、離れた場所に分散して設置する場合においても、複数の集線ユニットを安全に動作させることができる。また、集線ユニットは電源を有していないので、小型化することができ、配電線による接続によりフレキシビリティが向上し、壁に据え付けたり、弱電機器用ボックス内に収納したり、床に置いたりすることができ、様々な場所に容易に設置することができる。更に、外部電源の設置場所に依存されることなく情報配線システムを構築することができ、情報配線システムの増設および変更を容易に行うことができる。

【図面の簡単な説明】

【図1】本発明の一実施の形態における集線装置を示すブロック図。

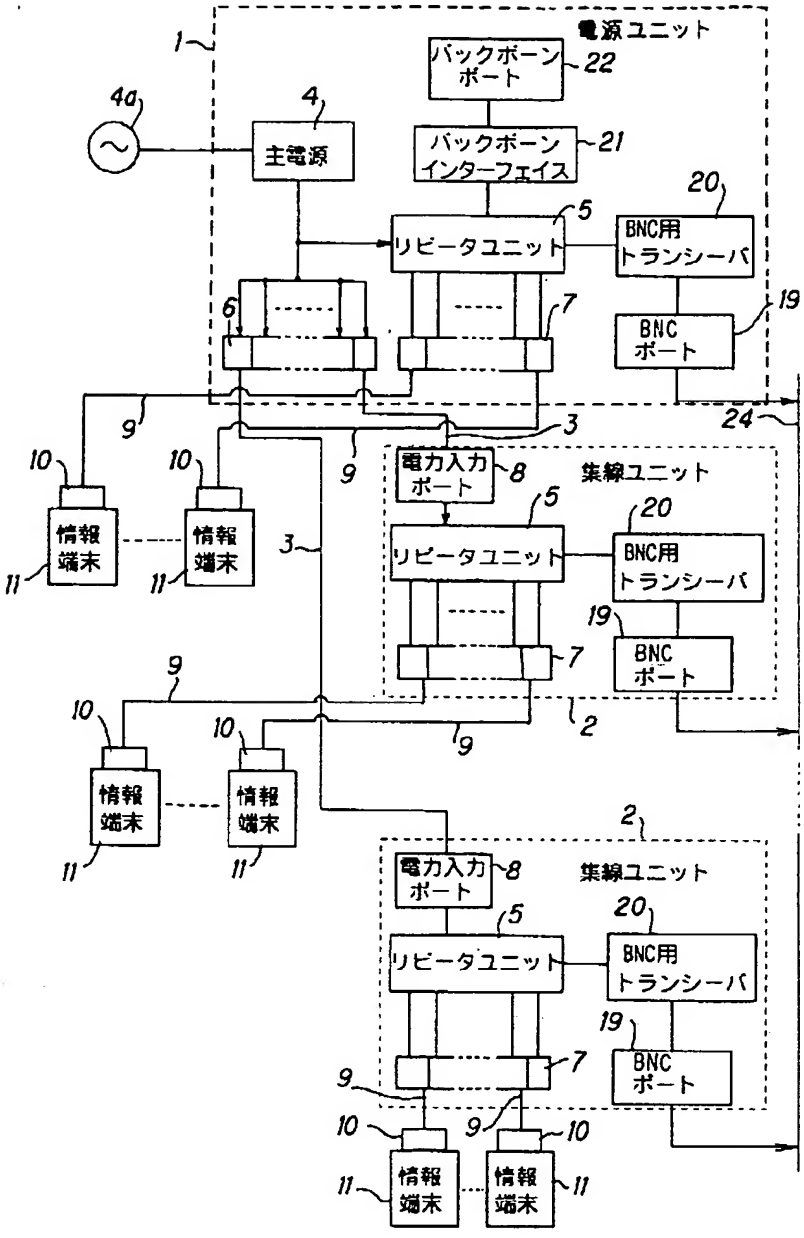
【図2】従来の集線装置を示すブロック図。

【図3】従来の集線装置を示すブロック図。

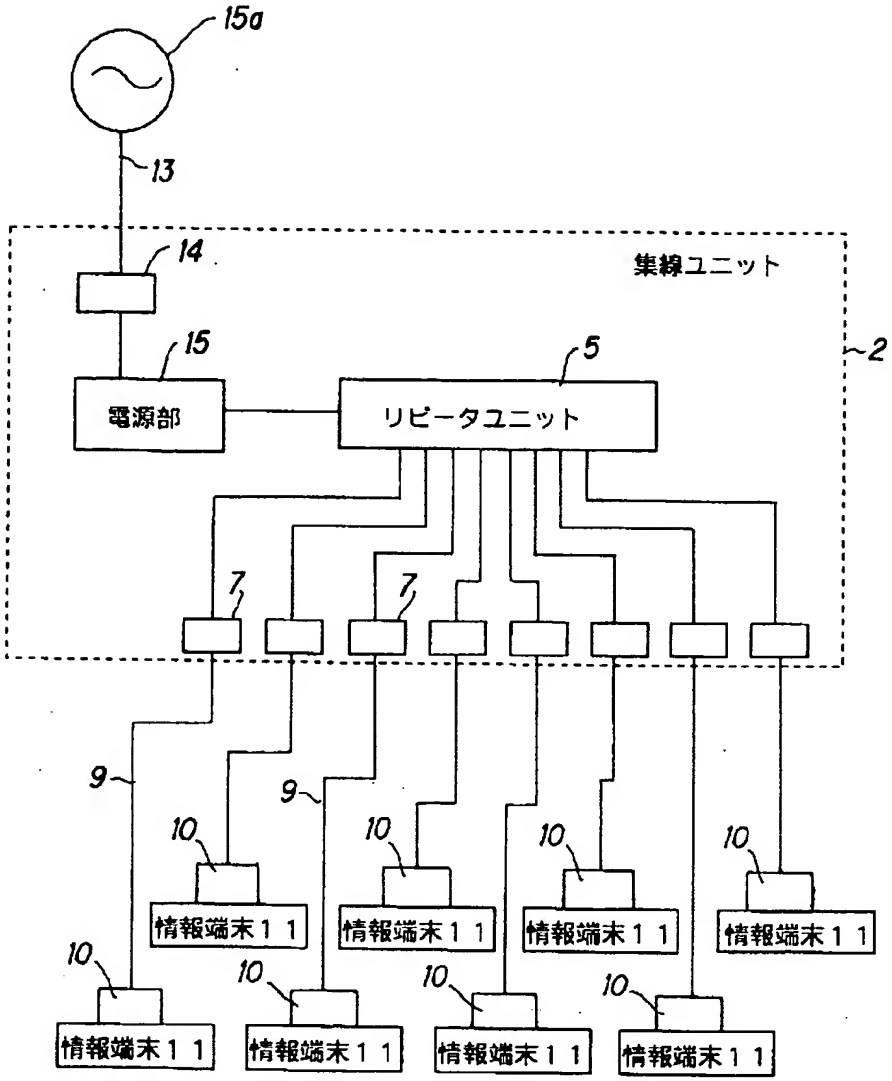
【符号の説明】

1　電源ユニット
2　集線ユニット
3　配電線
4　主電源部
5　リピータユニット
6　電力出力ポート
7　ツイストペアポート
8　電力入力ポート
9　ツイストペア線
10　TP-MAU
11　情報端末
19　BNCポート
20　BNC用トランシーバ
21　バックボーンインターフェース
22　バックボーンポート

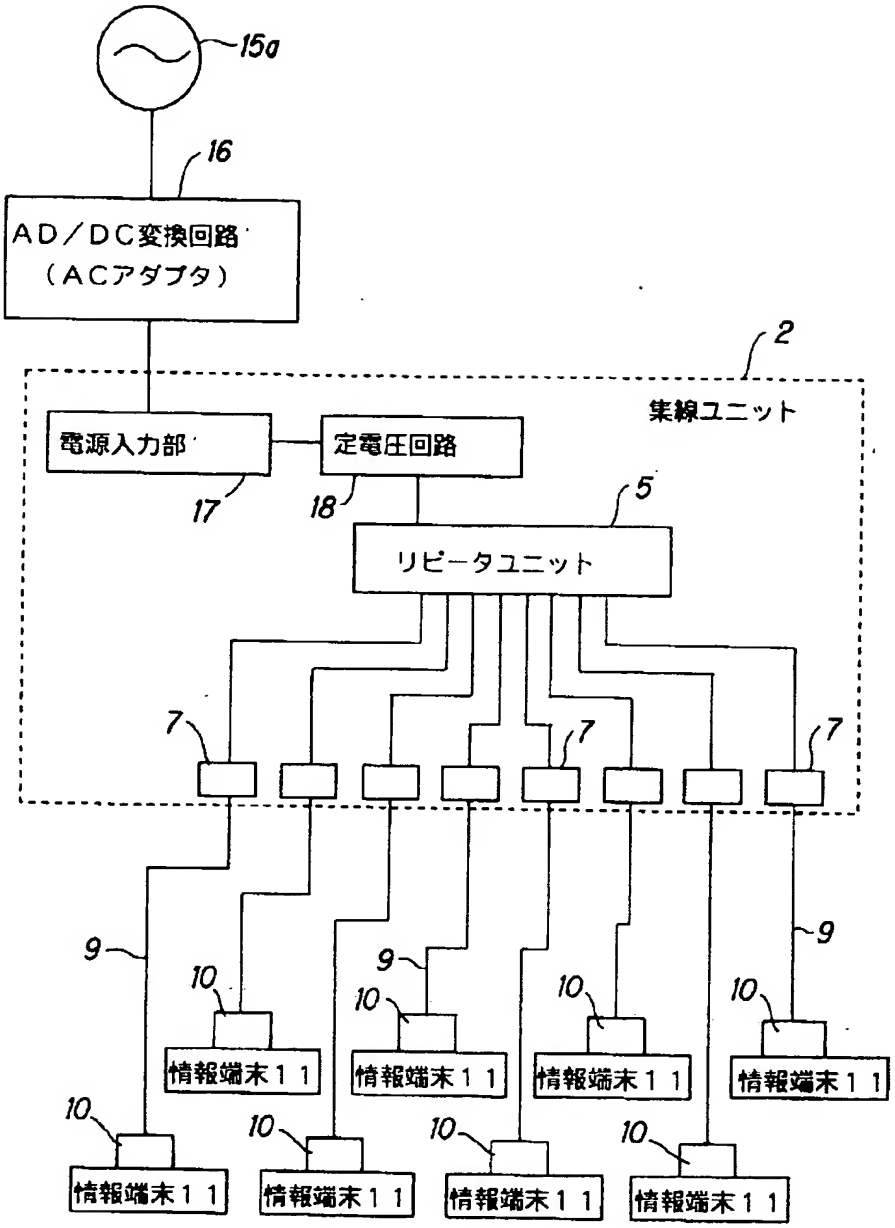
【図1】


電源ユニット
1
バックボーンポート
22
4a
4
主電源
バックボーンインターフェイス
21
20
5
リピータユニット
BNC用トランシーバ
6
7
BNCポート
19
24
9
3
10
情報端末
11
電力入力ポート
8
集線ユニット
2

【図２】


15a
13
14
集線ユニット
2
15
5
電源部
リピータユニット
7
7
9
9
10
10
10
10
10
10
10
10
情報端末１１
情報端末１１
情報端末１１
情報端末１１
情報端末１１
情報端末１１
情報端末１１
情報端末１１

【図３】



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